Sliding Mode Capacitor Voltage Control in Extended Commutation Cell based Inverter

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***Abstract*—An extended commutation cell (ECC) is a four-port four-switch power processing cell that allows for bidirectional energy transport in two orthogonal directions throughout the structure. By cascading multiple cells a high-quality output voltage waveform can be constructed with a high number of levels. The voltage across each cell capacitor can be adjusted independently of the load, resulting in a high flexibility in output levels. This paper derives a robust sliding mode control algorithm for capacitor voltage control in ECC based converters. It includes a cell current estimator, being intended for fast regulation of the internal states of each cell. The proposed method is analyzed, simulated and experimentally verified on a 4.4 kW eight-level inverter prototype.**

***Index Terms*—Buck-boost, sliding mode control, ECC, multi-cell, multilevel, switched capacitor.**

I. Introduction

With the rapid development of electronics one can find electric power converters, such as dc-dc and ac-dc converters almost everywhere. In the search for an increasing power density, the switching frequency is being raised and multilevel converters [1], [2] and modular converter structures [3]–[5] are being used, reducing the size of passive filtering components. Most popular examples of such multilevel/multicell converters are the flying capacitor converter, neutral-point clamped converter, cascaded cell multilevel converter and modular multilevel converter [6], [7]. A recent step in multicell and multilevel converters is the introduction of the ECC [8]. The single cell, as shown in Fig. 1 is composed of one capacitor, one inductor and four switches. Adding multiple cells in series results in a rapid increase in the number of levels, and adding cells in parallel enables single-fault safe operation. The application area of the ECC based inverter is in high performance, high reliability, such as precision industrial motor drives.

The circuit diagram of a converter with eight output levels is given in Fig. 2. Within each ECC the voltage of each capacitor can be controlled independently of the load connected [9]. Synthesis of an output waveform is realized by the (anti-) series connection of one or more capacitors. In order to have stable output voltage levels, the capacitor voltages should be accurately controlled. However, due to the buck-boost nature of the converter, it is difficult to control the local capacitor voltage with high dynamic performance over a wide range. Sliding mode control [10] is a non-linear control method that is used to control a system that can be represented by two or more different substructures. An electric power converter using switches is a system that can be represented as such, making it suitable to be controlled with sliding mode control [11], [12]. By using sliding mode control the internal capacitor voltage in a cell can be stabilized fast over a wide operating range, compared to conventional linear control.

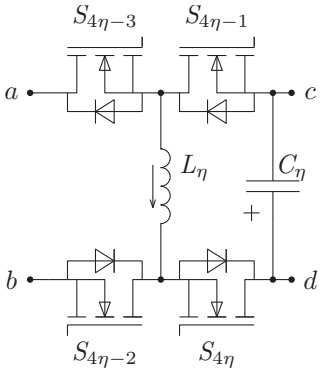

Figure 1. Basic circuit diagram of the extended commutation cell implemented with MOSFETs. Connection terminals are indicated with a, b, c and d.

This paper presents the analysis to obtain the control parameters for the sliding mode control of each cell. Next, a two-cell converter was simulated using the obtained control parameters and the stability is verified during operation. Finally, the simulated results have been verified in an experimental setup of a two-cell dc-ac converter of 4.4 kW.

II. Extended Commutation Cell

The basic ECC is shown in Fig. 1 where the connection terminals are indicated with letters a, b, c, and d. This basic cell is a voltage-to-voltage converter where terminals a and b are are supposed to operate as a pair, and, so are terminals c and d.

Operation of the ECC consists of two separate modes; the first mode is input-to-output direct connection, when switches $S_{4\eta-3}$ and $S_{4\eta-1}$ are turned on simultaneously, or when switches $S_{4\eta-2}$ and $S_{4\eta}$ are turned on. With the first pair of switches, terminal a is connected to c, with the second pair, terminal b is connected to d. The second mode is buck-boost operation, where energy can be transferred between a

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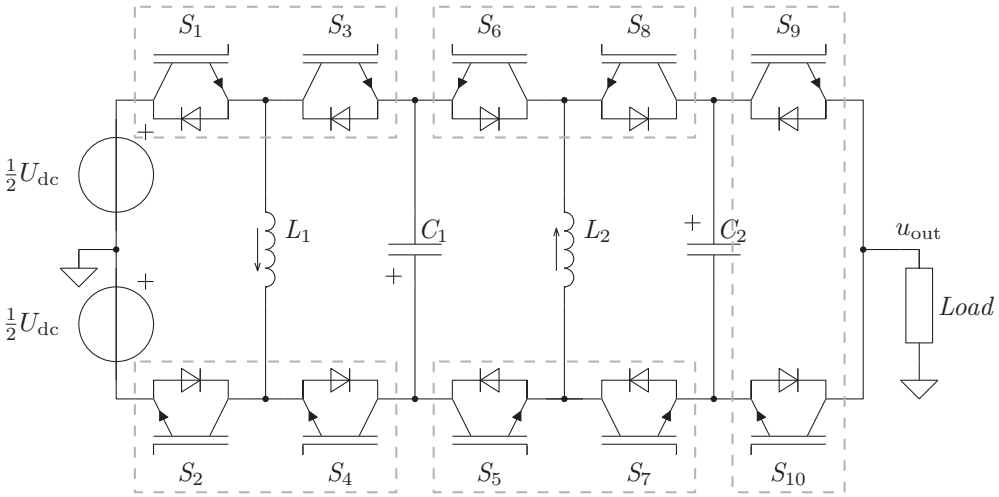

Figure 2. Circuit diagram of an ECC based eight-level converter, employing two ECCs and a half-bridge constructed with IGBTs.

voltage source connected to terminals a and b and the capacitor C_η. Assuming continuous conduction mode for the buck-boost operation, the capacitor voltage is given by

$$U_{C_\eta} = U_{ab}\frac{D_\eta^\perp}{1 - D_\eta^\perp} \tag{1}$$

where $D_\eta^\perp$ is the buck-boost duty ratio for $S_{4\eta-3}$ and $S_{4\eta-2}$, with $S_{4\eta-1}$ and $S_{4\eta}$ being complementary. The peak voltage across all switches in the switching cell is $U_{C_\eta} + U_{ab}$. Note that η is used as a generic identifier for an ECC.

The operation of the ECC, with both input-to-output direct connection and buck-boost combined, is shown in Fig. 3. With ideal components, these operating modes are fully decoupled.

A. N-Level converter

By using series connection of multiple ECCs, an N-level converter can be constructed, where N is exponentially related to the number of switches. A single ECC with a half-bridge gives a total of four output levels, adding a second ECC introduces an additional four output levels. The resulting two-ECC converter with eight output levels is shown in Fig. 2.

In an N-level converter, each additional cell multiplies the number of available output voltage levels by a factor of two. Therefore, the number of levels as a function of the number of ECCs, together with the two level introduced by the output half-bridge, is given by

$$N = 2^\sigma \cdot 2 = 2^{\sigma+1} \tag{2}$$

where σ is the number of cells cascaded in series. For a given number of cells the required number of switches, denoted by n_S, is found to be

$$n_S = 4\sigma + 2 \tag{3}$$

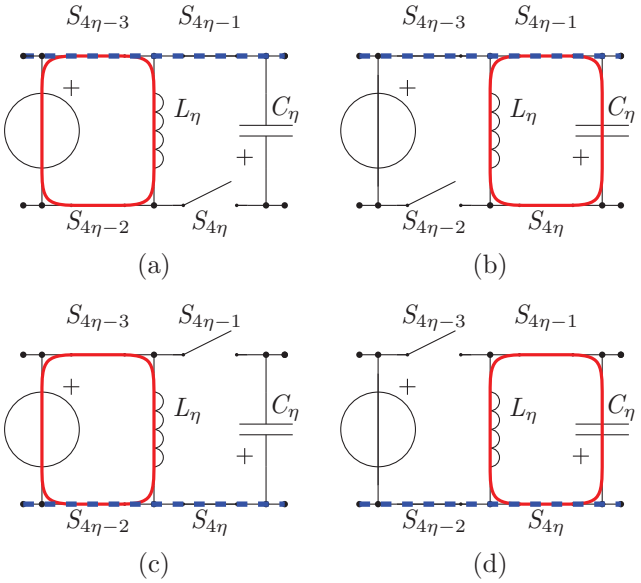

Figure 3. Combined ECC operation of input-to-output direct connection and buckboost operation. Dashed line: input-to-output direct connection path. Continuous line: buckboost path. Direct connection between a and c with buck-boost inductor connected to the input (a) and to the cell capacitor in (b). The other direct connection, between b and d is shown in (c) with inductor connected to the input and to the capacitor in (d).

B. Output levels

The output levels that can be achieved with the eight-level converter ($\sigma = 2$) from Fig. 2 are listed in Table I. Each of the levels is a combination of the input voltage source and the capacitor voltages U_{C_1} and U_{C_2}. As shown in [8], for a set of equidistant output levels, the capacitor voltage for C_η is given by

$$\frac{U_{C_\eta}(\sigma)}{U_{\mathrm{dc}}} = \frac{(-1)^{\sigma-\eta} + 2^{\sigma+1-\eta}}{(-1)^\sigma + 2^{\sigma+1}} \tag{4}$$

Table I
EIGHT-LEVEL CONVERTER OUTPUT VOLTAGE PER STATE

ℓ	u_{out}
4	$\frac{1}{2}U_{\text{dc}} + u_{C_1} + u_{C_2}$
3	$\frac{1}{2}U_{\text{dc}} + u_{C_1}$
2	$\frac{1}{2}U_{\text{dc}}$
1	$\frac{1}{2}U_{\text{dc}} - u_{C_2}$
-1	$-\frac{1}{2}U_{\text{dc}} + u_{C_2}$
-2	$-\frac{1}{2}U_{\text{dc}}$
-3	$-\frac{1}{2}U_{\text{dc}} - u_{C_1}$
-4	$-\frac{1}{2}U_{\text{dc}} - u_{C_1} - u_{C_2}$

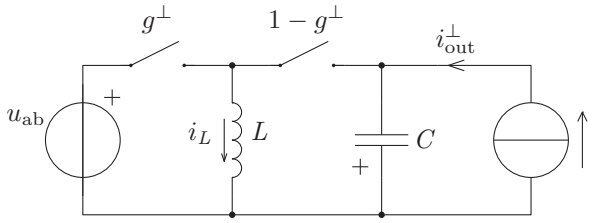

Figure 4. Basic buck-boost topology.

C. Voltage control

In Table I the set of output levels for a two-cell converter are presented. Since the levels are formed by directly connecting these capacitors in (anti-) series, stepping between levels results in significant load-steps for the buck-boost operation of the cell. This is first described in [13], where a load current correction method is used together with current mode control to provide a highly dynamic controller. Sliding mode control can also provide highly dynamic and robust behavior for power converters that operate by switching between two states. For each of the cells in the ECC based inverter, the buck-boost operation can be represented as such, and therefore provide high-performance control for the cell capacitor voltages.

III. SLIDING MODE CONTROL

Since the two operating modes in the ECC are decoupled, the buck-boost capacitor voltage control can be investigated separately from the output operation of the converter. Therefore the analysis for sliding mode control for the cell capacitor voltage is done on a simplified buck-boost circuit. The simplified circuit diagram of the buck-boost operation in a single ECC is given in Fig. 4. In the case $g^\perp = 1$ the left switch is conducting, if $g^\perp = 0$ the right switch is conducting. As a result the combined state space description is given by

$$\begin{bmatrix} \dot{i_L} \\ u_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_{\text{out}}^\perp \\ u_{\text{ab}} \end{bmatrix} + g^\perp \left(\begin{bmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\text{out}}^\perp \\ u_{\text{ab}} \end{bmatrix} \right) \quad (5)$$

Now constructing a vector with the state variables

$$\underline{x} = \begin{bmatrix} i_L \\ u_C \end{bmatrix} \quad (6)$$

a sliding surface can be conveniently defined as

$$\gamma(\underline{x}) = \left(u_C - u_C^*\right) + K\xi \left(i_L - i_L^*\right) \quad (7)$$

where u_C^* and i_L^* are the references for the capacitor voltage and inductor current respectively. Symbol ξ is a norm in ohms for K such that K is unit-less. Target is to define boundaries for $K\xi$ such that the system is stable, so

$$\lim_{t\to\infty} \left[\gamma(\underline{x}) = 0 \quad \text{and} \quad \dot{\gamma}(\underline{x}) = 0\right] \quad (8)$$

which means that ideally, for an infinite switching frequency, the system converges to $\gamma(\underline{x}) = 0$ in a finite amount of time.

The switch gating signal is dependent on the value of the sliding surface $\gamma(\underline{x})$. The most basic switch function to describe this relation, is a signum type of function, with

$$g^\perp = \begin{cases} 0 & \text{for} \quad \gamma(\underline{x}) \geq 0 \\ 1 & \text{for} \quad \gamma(\underline{x}) < 0 \end{cases} \quad (9)$$

Since the system must always converge to $\gamma(\underline{x}) = 0$, the derivative of $\gamma(\underline{x})$ must be such that the system will always return to the sliding surface. In a mathematical expression this means that

$$\dot{\gamma}(\underline{x}) \begin{cases} > 0 & \text{for} \quad \gamma(\underline{x}) < 0 \\ < 0 & \text{for} \quad \gamma(\underline{x}) > 0 \end{cases} \quad (10)$$

When writing (5) as

$$\dot{\underline{x}} = \underline{f}(\underline{x}) + g^\perp \underline{h}(\underline{x}) \quad (11)$$

the time derivative of $\gamma(\underline{x})$ can be written by

$$\dot{\gamma}(\underline{x}) = \nabla\gamma(\underline{x}) \cdot \dot{\underline{x}}^{\text{T}} = \nabla\gamma(\underline{x}) \cdot f(\underline{x})^{\text{T}} + g^\perp \nabla\gamma(\underline{x}) \cdot h(\underline{x})^{\text{T}} \quad (12)$$

where the gradient of the sliding surface is given by

$$\nabla\gamma(\underline{x}) = \begin{bmatrix} K\xi & 1 \end{bmatrix} \quad (13)$$

Combining (9), (10) and (12) the following set of requirements is obtained

$$\nabla\gamma(\underline{x}) \cdot f(\underline{x})^{\text{T}} < 0 \quad (14a)$$

$$\nabla\gamma(\underline{x}) \cdot f(\underline{x})^{\text{T}} + \nabla\gamma(\underline{x}) \cdot h(\underline{x})^{\text{T}} > 0 \quad (14b)$$

giving

$$\frac{1}{C}\left(i_L - i_{\text{out}}^\perp\right) - \frac{K\xi u_C}{L} < 0 \quad (15a)$$

$$\frac{K\xi}{L} u_{\text{ab}} - \frac{1}{C} i_{\text{out}}^\perp > 0 \quad (15b)$$

isolating K gives the following boundaries for K

$$K\xi > \frac{L}{C} \frac{i_L - i_{\text{out}}^\perp}{u_C} \quad (16a)$$

$$K\xi > \frac{L}{C} \frac{i_{\text{out}}^\perp}{u_{\text{ab}}} \quad (16b)$$

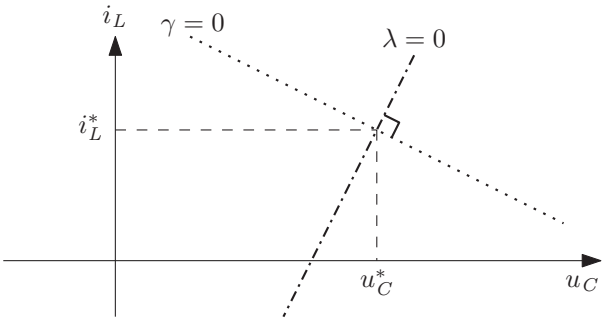

Figure 5. Sliding mode phase plane including sliding surface ($\gamma = 0$) and perpendicular surface $\lambda = 0$.

In steady state, when $\gamma \approx 0$ and $u_C \approx k u_{\mathrm{ab}}$ (where k is the buck-boost voltage gain), both requirements become

$$K\xi > \frac{L}{C}\frac{i_{\mathrm{out}}^{\perp}}{u_{\mathrm{ab}}} \tag{17}$$

as $i_L = i_{\mathrm{out}}^{\perp}(1+k)$. So for the steady state system, $K\xi$ should be chosen such that it always complies with (17).

A. Steady-state convergence

Now, for the ease of writing the errors for the capacitor voltage and inductor current are expressed as single symbols by

$$\begin{aligned} e_{\mathrm{i}_L} &= i_L - i_L^* \\ e_{\mathrm{u}_C} &= u_C - u_C^* \end{aligned} \tag{18}$$

To obtain the convergence to $e_{\mathrm{u}_C} = 0$ and $e_{\mathrm{i}_L} = 0$, or in short $e = 0$, the movement across the sliding surface must be determined. Therefore a surface is introduced which is placed perpendicular to the sliding surface γ. This surface is named λ and is given by

$$\lambda = \left(u_C - u_C^*\right) - \frac{\xi}{K}\left(i_L - i_L^*\right) \tag{19}$$

Graphically this is shown in Fig. 5. In order to obtain stable convergence to $e = 0$, without any sub-harmonic oscillations, the following primary stability criterion must be true

$$\lambda\dot{\lambda} < 0 \tag{20}$$

which is met when

$$i_{\mathrm{out}}^{\perp} < \frac{u_{\mathrm{ab}}}{K\xi}\left[\frac{C}{L}K^2\xi^2 + \frac{u_C - u_C^*}{u_{\mathrm{ab}} + u_C}\right] \tag{21}$$

In case $u_C < u_C^*$, the value of $K\xi$ must be higher to obtain convergence. Then the minimum value is given by

$$K\xi > \frac{L i_{\mathrm{out}}^{\perp} + \sqrt{L^2 {i_{\mathrm{out}}^{\perp}}^2 - 4Cu_{\mathrm{ab}}^2 \frac{u_C - u_C^*}{u_{\mathrm{ab}} + u_C}}}{2Cu_{\mathrm{ab}}} \tag{22}$$

in the worst case, when $u_C = 0$, (22) simplifies to

$$K\xi > \frac{L i_{\mathrm{out}}^{\perp} + \sqrt{L^2 {i_{\mathrm{out}}^{\perp}}^2 + 4Cu_{\mathrm{ab}}u_C^*}}{2Cu_{\mathrm{ab}}} \tag{23}$$

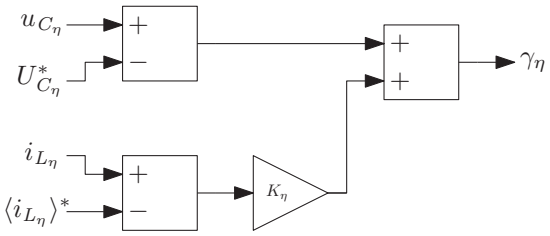

Figure 6. Sliding mode control implementation.

During steady-state operation the capacitor voltage will be close to the reference value, therefore (23) can be simplified to

$$K\xi > \frac{L}{C}\frac{i_{\mathrm{out}}^{\perp}}{u_{\mathrm{ab}}} \tag{24}$$

which is equal to (17) and therefore redundant.

B. Sliding mode control implementation

The implementation of the sliding mode controller in a simulation environment or prototype is shown in Fig. 6. The required references are an capacitor voltage set-point and inductor current set-point. Using the analysis from [13], the reference for the inductor current can be determined based on the output level and measured output current, for each cell and level as

$$\langle i_{L_\eta}\rangle^* = \mathbf{P}\begin{bmatrix}\underline{0} & \mathbf{I}\end{bmatrix}^{\mathrm{T}}\mathbf{A}\left(\mathbf{I} + \mathbf{K}^{-1}\right)\langle i_{\mathrm{out}}\rangle \tag{25}$$

with $\mathbf{I}$ being an identity matrix, and $\underline{0}$ a vector containing only zeros. Matrix $\mathbf{K}$, not to be confused with K, is a square matrix with the buck-boost gains on the diagonal. Additionally, $\mathbf{A}$ is an ancillary matrix describing the inter-cell buck-boost gain as

$$\mathbf{A}_{p,q} = \prod_{\eta=q}^{p} k_\eta \quad \text{if } p \geq q \text{ else } \mathbf{A}_{p,q} = 0 \tag{26}$$

and $\mathbf{P}$ is the level matrix, describing the contribution of each capacitor to the output voltage for every level. For a two-cell converter ($\sigma = 2$) this matrix $\mathbf{P}$ is given as

$$\mathbf{P} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & -1 \\ -1 & 0 & 1 \\ -1 & 0 & 0 \\ -1 & -1 & 0 \\ -1 & -1 & -1 \end{bmatrix} \tag{27}$$

The term $\langle i_{\mathrm{out}}\rangle$ in (25) indicates the switching periodic average of the output current, taken over the switching period of the direct input-to-output operation, indicated with $T^{\vdash}$.

By subtracting the calculated inductor current reference from the momentary inductor current, a zero reference can be used for the inductor current in the sliding mode controller. To limit the switching frequency a fixed hysteresis switching

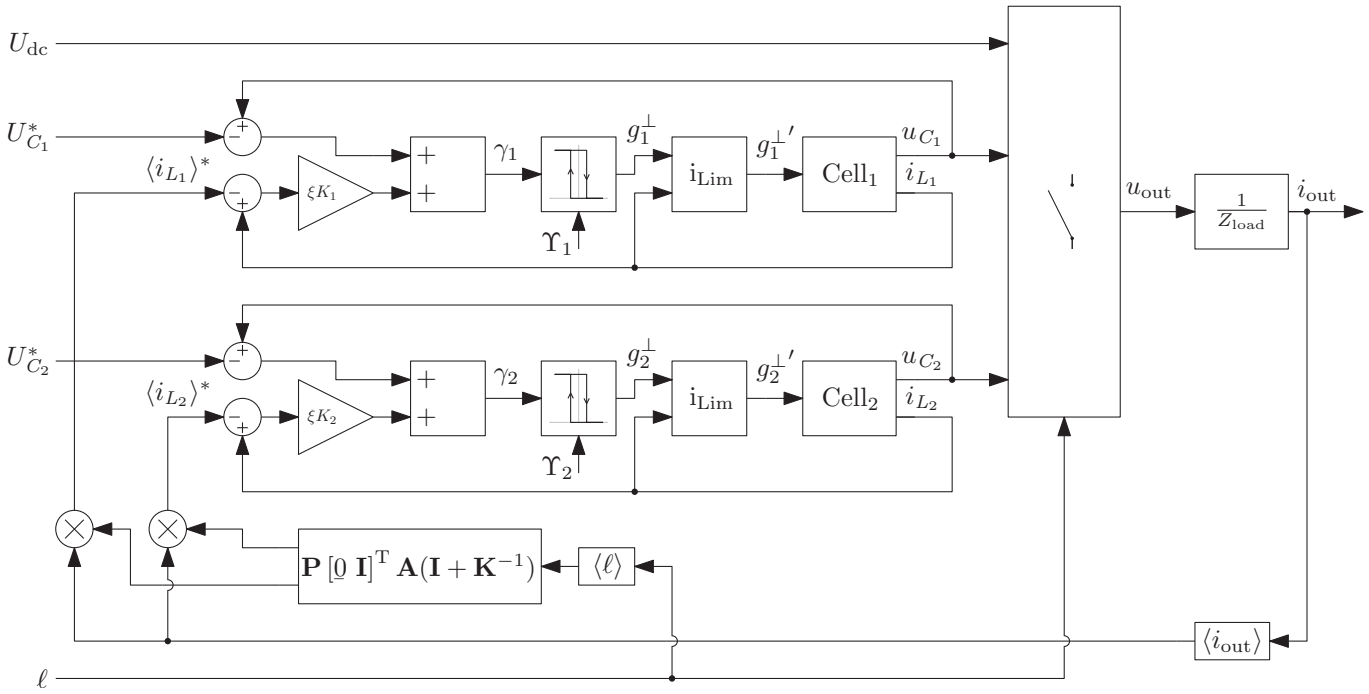

Figure 7. Implementation of sliding mode control in two-cell ECC based dc-ac converter.

Table II
TWO-CELL, EIGHT-LEVEL DC-AC CONVERTER EXPERIMENTAL SETUP PARAMETERS

Parameter	Value	Parameter	Value
$U_{\rm dc}$	300 V	$f_{\rm sine}$	50 Hz
$U_{\rm out}$	230 $\mathrm{V_{rms}}$	$f_{\rm sw}^{\vdash}$	10 kHz
$\hat{u}_{\rm out}$	$\pm$350 V	L_1, L_2	210 μH, 140 μH
$U^*_{C_1}$, $U^*_{C_2}$	100 V	C_1, C_2	1000 μF
$I_{\rm out}$	19 $\mathrm{A_{rms}}$	$P_{\rm out}$	4.4 kW

function can be used. An overview of the control system of a two-cell converter with a fixed hysteresis is shown in Fig. 7. The extended commutation cells are indicated with a ECC_η block. To have controlled startup behavior an robust operation a hysteresis current limiter is added, indicated with $\mathrm{i_{Lim}}$.

IV. EXPERIMENTAL RESULTS

In order to test the sliding mode control algorithm with the obtained criterion for stability, a two-cell eight-level dc-ac converter of 4.4 kW is simulated and experimentally verified. The parameters of the converter are given in Table II.

A. Simulated waveforms

Based on the parameters of the experimental setup, a simulation model was implemented to verify the sliding mode control algorithm. The sliding mode control constant K in (17) was chosen equal to $5K_{min}$, where the value of K_{min} is obtained for the worst-case operating conditions. The simulated converter was operated at a quasi-constant inductor current ripple, the cell output current was determined using the measured load current. The resulting waveforms, including the output voltage, output current, capacitor voltage and inductor current are shown in Fig. 8. A slight variation in the current ripple through the inductor is visible. This is caused by the hysteresis of the inductor current in combination with the ripple in the output current.

B. Power stage

The two-cell prototype converter, with circuit diagram as shown in Fig. 2, consists of five Semikron SKM100GB12T4 half-bridge IGBT modules with isolated drivers. The values of the inductors were dimensioned such that, at the same switching frequency, the nominal current ripple is the same for both inductors. The inductors are constructed around a core of four Magnetics K133TC026 sections each. Electrolytic capacitors were selected as cell capacitors and are chosen for their rms current rating. Parallel to the cell capacitor, film snubber capacitors were placed close to the power modules. The currents in the inductors were measured with high-frequency current transducers, the capacitor voltages were measured using isolated voltage transducers.

C. Controller implementation

The control system, shown in Fig. 7, was implemented in a dSPACE system composed of a DSP and FPGA subsystem. The output reference signal $u^*_{\rm out}$ was generated in the DSP and the phase-disposition PWM modulator for the multilevel output signal was implemented in the FPGA. The output was operated in open-loop and works as a variable voltage source. The sliding mode controllers were implemented entirely in the FPGA, using high frequency ADCs (10 MHz) to sample the inductor current and capacitor voltage.

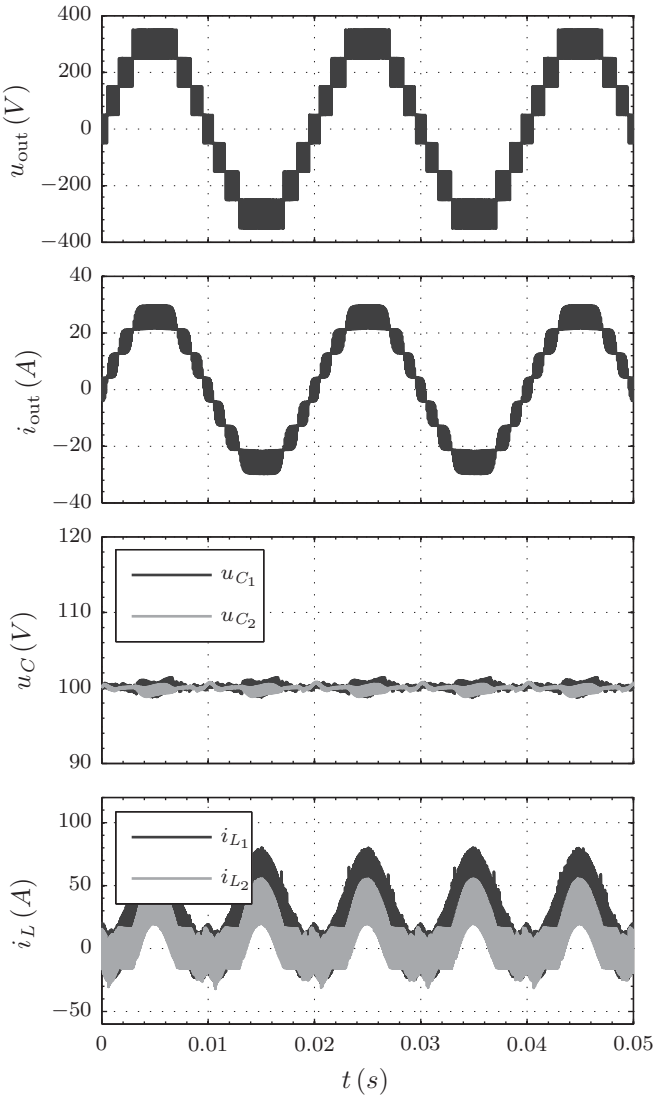

Figure 8. Simulated waveforms of two-cell dc-ac converter operating with $I_{\text{out}} = 19$ A, showing the output voltage u_{out}, output current i_{out}, capacitor voltages, and inductor currents.

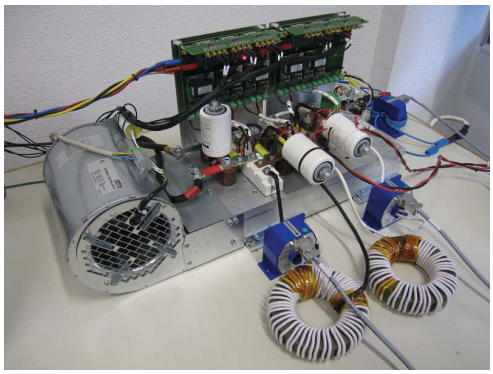

Figure 9. Experimental setup.

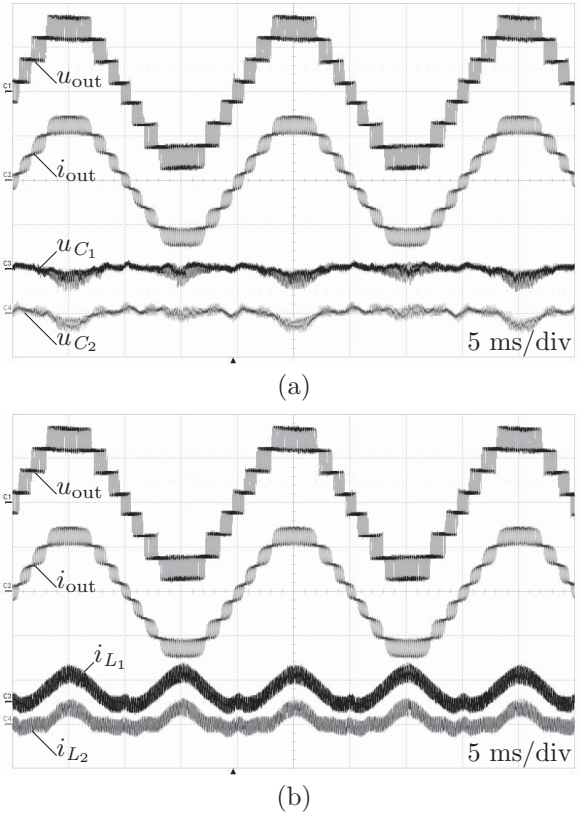

Figure 10. Experimental results of two-cell, eight-level converter operated at 230 V_{rms}, 50 Hz waveform with an output current of 19 A_{rms}. Output waveforms and capacitor voltage (a) and inductor currents (b). Output voltage u_{out} (200 V/div), output current i_{out} (20 A/div), capacitor voltage ripples (10 V/div), and inductor currents (100 A/div).

D. Measurement results

The completed experimental prototype is shown in Fig. 9. A symmetric supply of 150 V is used to power the converter and the load is formed by an 11.7 Ω power resistor R_l with a parasitic inductance L_l. Due to the switching delay of the IGBTs, a blanking time is added to the gating signals. This blanking time is 1 μs and was implemented as a delayed-on for each switch. The output reference is a sine wave of 50 Hz with a modulation depth of 0.9.

The obtained measurement results, where the prototype converter was operated with a load current of 19.2 A_{rms}, are shown in Fig. 10. The operating conditions are identical to the simulations of Fig. 8. In Fig. 10 (a) the output voltage and current, together with the capacitor voltage ripples are given. The output shows a clear eight-level waveform where the grey area between the levels is caused by the pwm of the output voltage. The inductor currents are plotted in Fig. 10 (b) with the same time scale.

The ripple in the capacitor voltage is slightly larger than in simulation but the waveform is comparable. A slight decline is visible in the output waveform which is caused by a 50 Hz voltage ripple on the power supply midpoint. The sliding mode controller proves to be stable from zero current, at the zero crossings, to the maximum output current. Compared to

conventional current mode control used in [9], the ripple was significantly reduced. However, when using the output current information as done in [13], the capacitor voltage ripple is in the same order of magnitude.

V. Conclusions

In this paper a sliding-mode control structure was proposed to be applied to extended commutation cell based high performance inverters, aiming at fast stabilization of the converter internal voltages. The converter was analyzed and a robust set of control parameters was proposed together with an estimator for the inductor current references. The obtained parameters have been confirmed by detailed simulation and were experimentally verified on a two-cell converter prototype.

The experimental verification shows only a small ripple in the capacitor voltage, which is significant improvement over conventional current control. However, when using current control with load current correction, the ripple is in the same order of magnitude.

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